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Synopsys and STMicroelectronics

STMicroelectronics Successful Deployment of Synopsys Embedded Memories Diagnosis Flow for Advanced Technology Nodes

"With the introduction of new process technologies, it is critical for STMicroelectronics to enable test, repair and bitmapping of embedded memories used in System on Chip (SoC) applications. The Synopsys STAR Memory System (SMS) enabled comprehensive memory debug and diagnosis on FinFET and planar technologies, identifying and accelerating application of corrective actions."

~Roberto Gonella, Executive Director, STMicroelectronics

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Overview

STMicroelectronics designs complex Systems on a Chip (SoC) in advanced technology nodes for market segments such as enterprise, networking, MCU and high reliability automotive. These products are designed with thousands of memory instances with very high-quality standards. The production goals are to accelerate cycle time in the New Product Introduction (NPI) phase and shorten turn-around-time in failure analysis when defective parts with embedded memories are detected.
Synopsys STAR Memory System™ is used to test, repair and diagnose embedded memories while Synopsys Yield Explorer performs analytics on memory diagnostic data to help quickly identify and resolve systematic failure mechanisms for the most advanced process nodes. The combined solution is a key enabler for STMicroelectronics to introduce new SoCs to the market with the latest process technologies.

Challenges

- Thousands of embedded memory instances covering 40 to 80% of the total SoC area
- New and complex fault types associated with advanced process technologies
- ISO26262 certified memory test and repair solution to meet high-reliability test and diagnosis criteria
- Minimal design impact of DFT logic
- Leverage industry-standard interfaces and minimize Automated Test Equipment (ATE) time for testing
- Rapid generation of production-ready test patterns and easy-to-use bitmap flow
- Fast and precise fault isolation to enable process fix and maintain the production ramp-up pace

"At STMicroelectronics, we believe that an effective diagnosis solution facilitates an easy and intuitive usage for SoC yield analysis engineers. The seamless interoperability of the Synopsys products (SMS, Yield Accelerator, and Yield Explorer) allowed us to benefit from an automated flow."

~Nelly Feldman, Senior Diagnosis Expert, STMicroelectronics

Synopsys Solution

STMicroelectronics deployed Synopsys Star Memory System (SMS), Synopsys SMS Yield Accelerator, and Yield Explorer to enable an automated memory diagnostics and debug flow combining test pattern creation, the failing bitmap data generation, statistical analysis, and identification of candidates for physical failure analysis.

The Synopsys SMS diagnosis flow played a key role in the rapid qualification of SoCs developed in FinFet technologies for complex ASICs. Despite challenging failure modes, Synopsys SMS achieved a high success rate for failure analysis.

The Synopsys SMS flow deployed across multiple design environments and product groups at STMicroelectronics, consistently delivered physical failure analysis results with a high degree of accuracy.

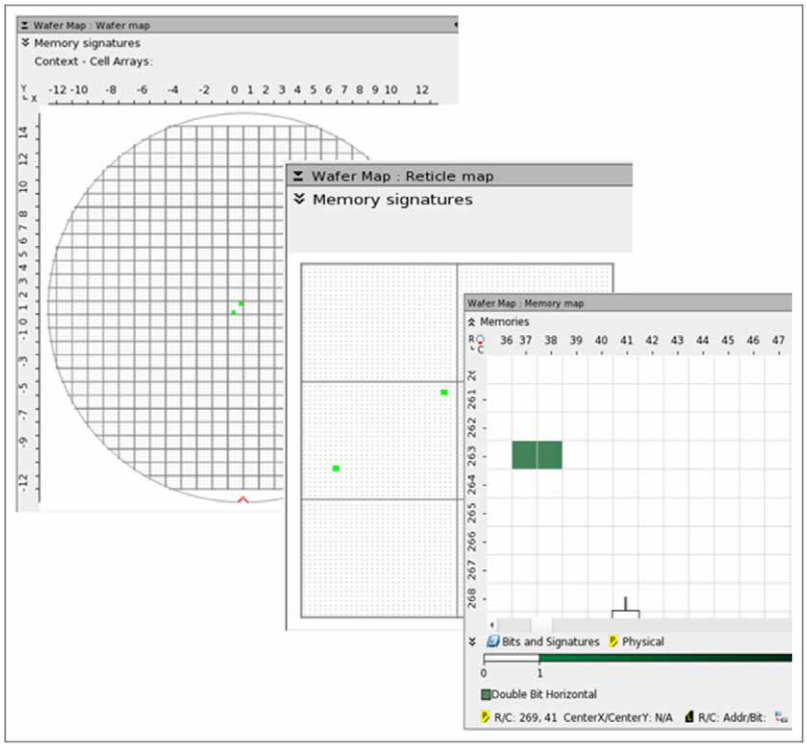

Figure 1: SMS Yield Explorer failing bit identification

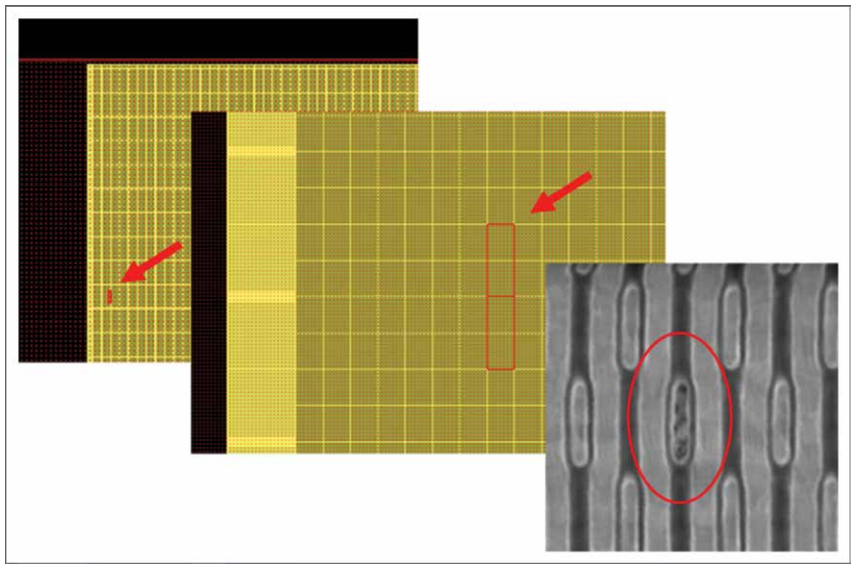

Figure 2: Physical failure layout mapping to silicon with physical root cause of the electrical failure

Key Benefits

Synopsys Star Memory System (SMS) enabled:

- High-quality test to provide full memory defect coverage with minimum test time
- Efficient on-chip repair across multiple operating PVT corners and frequencies
- Hierarchical architecture with automated SoC integration and verification
- ISO26262 certified ASIL-D (Automotive Safety Integrity Level) for random and systematic faults to cover the most stringent safety considerations

Synopsys SMS Yield Accelerator offered:

- Simplified generation of test vectors for ATE (Automated Test Equipment)
- Superior diagnostics capabilities with an exact match of failing bits and physical coordinates identification
- Silicon test results-based fault analysis and root-cause guidance

Synopsys Yield Explorer provided:

- Statistical and data analysis with wafer and test visualization capabilities
- Complex data sources interconnection to allow correlations across site-parametric, design, physical verification, simulation and product test
- Synchronized Component Architecture to integrate all incoming data into a single, coherent analysis framework
- Interactive use-case flow between chart and spreadsheet windows, wafer maps, failing net, and layout
- Dynamically extendable data model to bring in any custom data fields into the database

R&D Expertise and Technical Support

STMicroelectronics has a long-standing collaboration with Synopsys in the diagnosis domain. The Synopsys SMS, SMS Yield Accelerator, and Yield Explorer product teams successfully enabled the implementation of a complete diagnosis flow for embedded memories. Support for key diagnosis steps such as bitmap pattern generation, bitmap analysis, and candidate selection for physical failure identification helped achieve STMicroelectronics's target goal of improved turn-around-time in NPI and ramp-up.

> *"Integrating Synopsys diagnosis suite for memories is a win-win, not only for STMicroelectronics and Synopsys, but also for STMicroelectronics clients who can count on the reliable, timely support while introducing and qualifying new products in advanced technologies."*
>
> ~Roberto Gonella, Executive Director, STMicroelectronics