Influence of Ti-Al(Cu) backend layer scheme on repetitive-power-pulsing robustness

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***Abstract*—This study explores impact of layer scheme and thicknesses in Ti-Al(Cu) backend-stack variants of smart-power integrated circuits on reliability under repetitive power pulsing operation. We investigate the robustness of output driver stages with accelerated end-of-life testing and discuss lifetime modelling to derive design guidelines, e.g. for valve drivers in automotive application. Three backend-stack variants of different AlCu film thickness and Ti/TiN barrier-layer scheme are compared. The highest robustness in terms of time to failure is obtained using a stack of thin AlCu metal layers formed by a non-reactive Ti/TiN stack. Respective aging mechanism is explored by failure analysis and the trade-off with current density capability of the backend-stack is discussed.**

***Index Terms*—power transistors, active cycling, reliability, accelerated aging, titanium compounds**

I. Introduction

While usage of full-copper backend-of-line (BEOL) configuration with low-k dielectrics is established for advanced node integrated circuit (IC) technology, the classical aluminum metallization system still finds broad usage in smart-power designs for automotive and industrial applications. Typically integrated with a highly conductive top copper layer, here the AlCu metallization stack has to provide elevated current and voltage capability for harsh mission profiles of the product while high frequency performance is not critical. Transition to full-Cu BEOL and assessment of benefits vs. integration costs and reliability challenges is matter of current development activities [1], [2], [3]. In particular, usage of integrated power stages as low-side switches to control inductive loads, e.g. magnetic valves, represents a very harsh application mode for the BEOL in automotive ICs [4]. Here the power stage has to dissipate the induced power during switch-off, leading to a pronounced short increase of local device temperature for each switching cycle (fig. 1), so called repetitive power cycling (RPP) operation. For discrete power devices, these thermomechanical stress cycles lead to pronounced aging of the usually thick top aluminum metal layer itself [5]. In comparison, for smart-power IC products additional failure channels exist: The strong temporary lateral temperature gradient induced from the RPP stress cycle leads to severe mechanical stress on the IC backend structures due to the mismatch of CTE of aluminum or copper metals and dielectrics which may cause degradation and IC failure in respective applications [6]. The challenge for IC design is to guarantee safe operating life for a given mission profile which may involve billions of cycles [4] with minimized consumption of silicon area. Thus for a given IC technology a dedicated RPP characterization activity to assess BEOL robustness against RPP stress is needed. Previous works have described the failure mechanism in BEOL and proposed an aging model based on Coffin-Manson approach [7], [8], identified the influence of AlCu thin layer thickness in experiment and simulation [6], [9], compared AlCu BEOL robustness with dual damascene copper BEOL stack [3], and proposed optimized device design and control schemes to reduce RPP stress [10], [11].

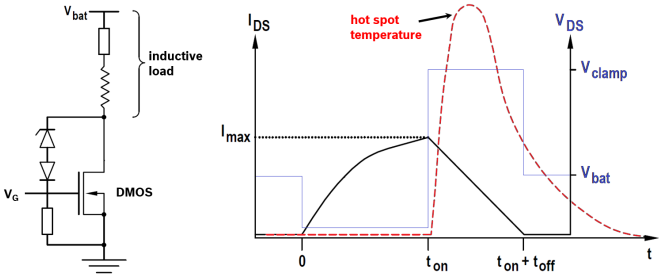

Figure 1. Power stage (DMOS) used as low-side switch in clamped inductive switching configuration. Right: Sketch of drain voltage (blue line), current (black line), and hot-spot temperature (red-dashed line) of the power stage versus time for a switching cycle.

Mainly based on an empirical end-of-life (EoL) test approach we investigate and model RPP-robustness of Ti-Al(Cu) BEOL variants for smart-power ICs using dedicated test structures. In particular, we study the influence of AlCu layer thickness and Ti/TiN barrier-layer scheme, since the latter has not been addressed in previous works. In the context of smart-power applications, additionally we discuss the trade-off between RPP robustness with current density capability.

II. Test Structure Design and BEOL Layer Scheme Variation

The test structures have been derived from application-near designs of 40V and 60V nLDMOS output driver stages in current Bipolar-CMOS-DMOS (BCD) technology. A planarized

AlCu metal stack with tungsten plugs and top-Cu power routing distributes the power pulses to drain and source region of the typically 0.5mm² large power stage. Thickness of AlCu layers is in the range from 400nm to 900nm. Similar test devices (DUTs) have been processed with different BEOL variants, such that we can compare RPP robustness of BEOL layer scheme without layout design influence. In a typical clamped inductive switching configuration, every test structure contains beside the main driver a chain of Zener-diodes between drain and gate to limit drain-source voltage V_{DS} and to control gate voltage during power pulse automatically (see fig. 1). Within this V_{DS}-clamp, the DUT operates at a point of high power dissipation. To draw off gate charge after the power pulse, a pull-down resistor between gate and source is included, too. Optionally the structures also contain up to four tightly embedded NPN-type temperature sensors used to measure transient temperature locally in the active area during the pulse event [12] (comp. fig. 2a).

To analyze local current density, power density and temperature distribution in the metal routing of the power stage, we execute electrothermal simulations using the electrothermal solver ETHAN from Silicon Frontline Technology Inc [13] (comp. fig. 2b-d). It allows a self-consistent transient solution of the current flow in the multi-finger metal stack and power dissipation in the active area of the power stage based on local device operation point and temperature. The thermal boundary conditions of the simulator as well as the temperature sensor readouts were calibrated before under well-known test conditions [14]. We can thus transfer thermal stress conditions, i.e. resulting peak temperature and temperature distribution, to test structures without temperature sensor, e.g. power stages of given products.

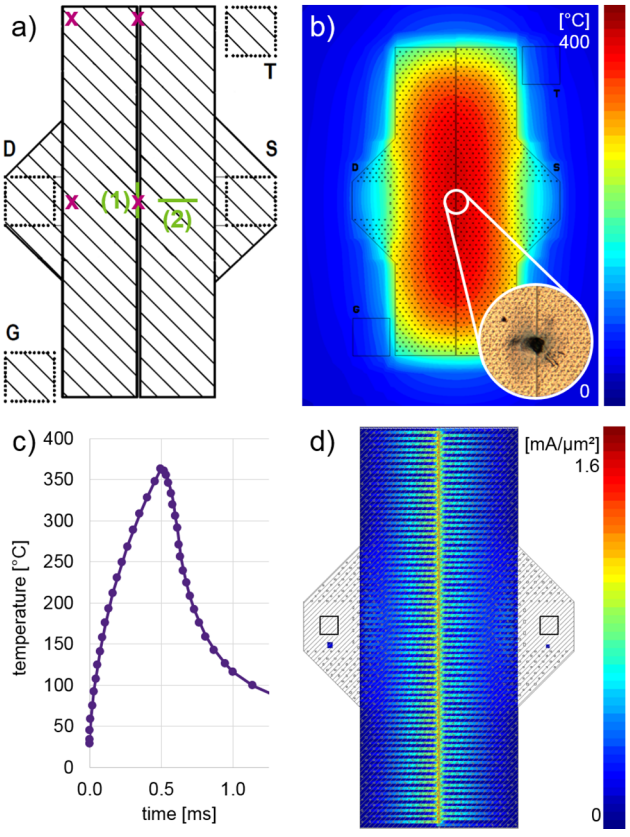

Figure 2. DUT overview and electrothermal simulation results for a rectangular power pulse: (a) Top view of the dedicated test structure based on a nLDMOS with overall device size of typically 0.5mm² and two big Cu-plates distributing power to drain and source fingers. Crossmarks indicate position of embedded temperature sensors. The green lines indicate the two FIB cuts for cross section analysis (section IV). (b) Simulated temperature distribution at t = 0.5ms at active silicon surface (comp. (c)). The inset shows image of typical failure signature after RPP EoL test. (c) Simulated temperature curve at active silicon surface in the center of nLDMOS area, ΔT = 350K. (d) Simulation of the lateral current distribution of the uppermost AlCu metal level at t = 0.5ms.

For the results discussed here, RPP end-of-life (EoL) trials have been executed applying rectangular power pulses to the DUTs. Those are practically much easier to control compared to using real inductive or dedicated electronic loads to generate triangular pulses like in application [15], [16]. With respect to peak temperature for each event and for RPP lifetime results, we have observed good agreement for both pulse shapes when mapping the energy and length of the rectangular power pulses to the triangular ones. Stress tests have been done both using packaged devices for long running trials and tests on wafer level for highly accelerated tests [14]. For the latter we use a Keithley 2430 1kW pulsed mode SourceMeter within an automated setup on a semiautomatic probe station, delivering bursts of millisecond rectangular power pulses of typically 0.5ms length and 100Hz pulse period at ambient temperature 25°C if not stated otherwise. For failure detection, the V_{DS} leakage in off-state and V_{DS}-value under pulsing is monitored.

Three AlCu BEOL variants A, B, and C have been investigated, which are related to current smart-power technology requirements for automotive mission profile with high temperature operation. The thin metal stack has to provide both densely routing capability for low-voltage digital part of IC and to support low-resistive routing for integrated driver stages between active device array and top power metal for up to several amps. Reduced current density to improve lifetime with respect to electromigration (EM) limits can be obtained by using multiple thin metal layers in shunted configuration or by increasing the layer thickness of the upper layers in the AlCu stack. Additionally it is known that EM robustness of AlCu layers of given thickness itself can be improved by the Ti/TiN barrier-layer scheme [17], [18].

The variants A, B, and C reflect these options for the AlCu BEOL stack (see fig. 3): As reference, we tested a stack A with a thicker uppermost AlCu metal level compared to the lower ones. For the variant B, in comparison, prominently the uppermost AlCu metal layer thickness has been reduced. To improve process stability and adhesion between the applied layers, additional Ti and TiN layers were implemented, too. The third variant C uses nominally equal AlCu metal thickness as B but here the AlCu layers are directly embedded in thicker bottom and top Ti layers. After an annealing step during process flow, this configuration results in the formation of a $TiAl_3$ coat, whereby the AlCu core cross section of the metal level is reduced slightly. Because of alloy formation during annealing step, which is done after every metal level deposition, this Ti/TiN-Al configuration is also called reactive stack instead of the non-reactive stack of variant B. The reactive Ti/TiN layer approach is known to enhance EM robustness and thus current capability

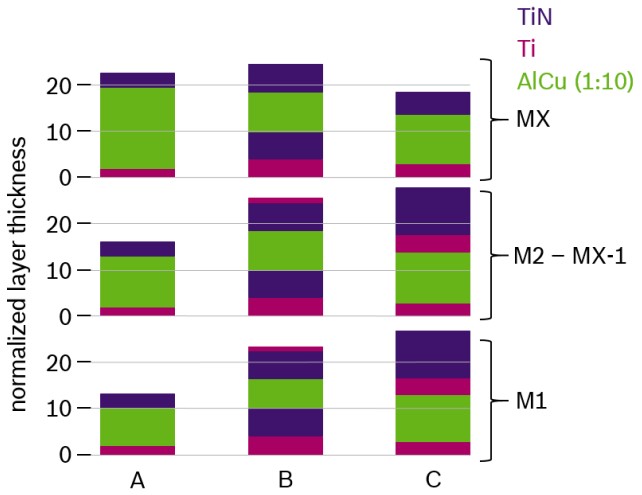

Figure 3. Schematic comparison of deposited material layer sequences before annealing for the metal levels M1 - MX (MX: uppermost thin metal level) of the three BEOL stacks. Thickness of main AlCu film is scaled 0.1x compared to barriers.

for variant C compared to variant B for similar layer thickness. In this regard, stack A may be called half-reactive, having a relatively thin lower Ti layer directly below the main AlCu film.

III. RPP ROBUSTNESS COMPARISON

The RPP EoL test results for our reference BEOL stack A are shown in fig. 4. As stress variables generally the pulse power, pulse length, and the basis junction temperature T_j may be varied. For fixed pulse length, a higher pulse power corresponds to a higher thermal swing ΔT per pulse. Fig. 4a shows test results at T_j = 75°C for three different ΔT analyzed with Weibull failure distribution. The mean number of pulses to failure N_f (t63%) increases strongly with decreasing ΔT, the values of Weibull slope are in the range of 3 to 7. For all the trials reported DUT failure occurs spontaneous as a (catastrophic) short in the metal routing stack of the drivers, which we confirmed by failure analysis. For the DUTs of the given technology, no relevant parameter drift is detectable before failure.

For the EoL data of stack A we find that mean RPP lifetime N_f can be modeled for a wide range of T_j and ΔT with a modified Coffin-Manson (CM) model based on the Norris-Landzberg-ansatz [19]:

$$N = A \cdot (\Delta T)^{-n} \cdot exp\left(\frac{E_a}{k_b\left(T_j+\frac{\Delta T}{2}\right)}\right) \qquad (1)$$

with technology-related constant A, CM-exponent n, and activation energy E_a. Fig. 4b shows the model fit together with the EoL data for a subset of trials, where error bars relate to uncertainty in the experimental thermal conditions on wafer and package level and to the width of the Weibull distribution, respectively. For the CM exponent and the activation energy we obtain values of n ~ 7 and E_a ~ 0.5eV.

Generally, we would expect the simplified empirical CM model to hold for the low-cycle regime of RPP stress at very high ΔT per pulse. In this case, the strong lateral temperature

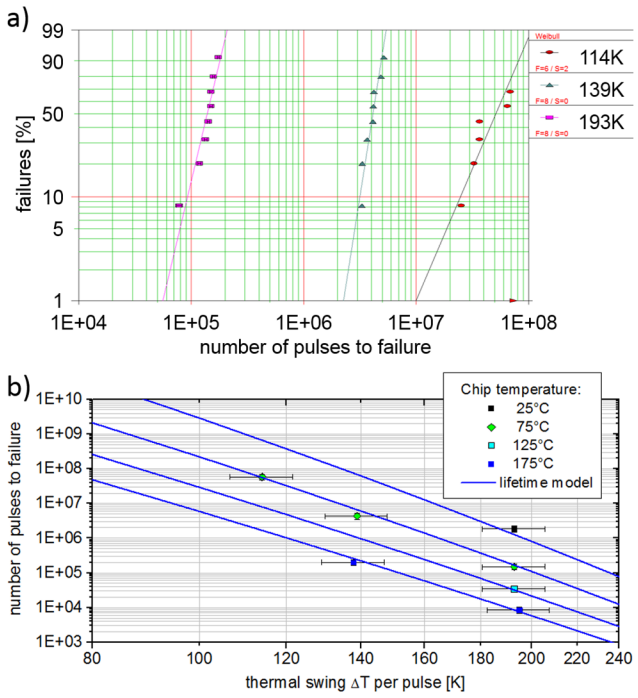

Figure 4. RPP EoL results for backend variant A: (a) Weibull distributions for trials at junction temperature T_j = 75°C with varied thermal swing ΔT. (b) Double logarithmic CM chart: The points indicate the mean RPP lifetime of a representative group of dedicated test structures at different basis junction temperatures. The lines represent the adapted modified CM model.

gradient across the driver stage (comp. fig. 2b) leads to a degree of stress on the IC backend structure due to the mismatch in CTE of metals and dielectrics, which is assumed to exceed the (temperature dependent [20]) yield point of the metal layers. Such, each cycle can accumulate a viscoplastic deformation of the metal and ultimately, stress on dielectrics may exceed critical limits. Then DUT failure occurs indicated by an electrical detectable leakage path or even short in the drain/source metal path of the driver, which was confirmed by failure analysis. The high value n = 7 found for the CM exponent, fits into this picture, indicating a brittle material fatigue [21].

For the BEOL stack A, however, we find the CM-trend to hold over almost five orders of magnitude in RPP lifetime, although Weibull slope becomes slightly lower for the longer lifetime trials. Considering also influence of T_j and pulse length this allows straightforward derivation of design guidelines for different RPP mission profiles, e.g. for anti-lock braking systems or injection valve drivers. In addition, we can use highly accelerated trials in a meaningful manner to give feedback on RPP robustness and integrity of BEOL, even on wafer [14].

The influence of the variation in backend-stack B and C compared to A, we investigated in the low-cycle regime as well: Fig. 5a shows the thermal swing per pulse needed to reach EoL for a fixed condition of roughly 1M pulses to failure for the three stack variants, with T_j = 25°C. Compared to our reference stack A, where ΔT ~ 200K leads to mean lifetime of 1M pulses, both for stack B and stack C a much higher thermomechanical load is needed for devices to fail after approx. 1M pulses.

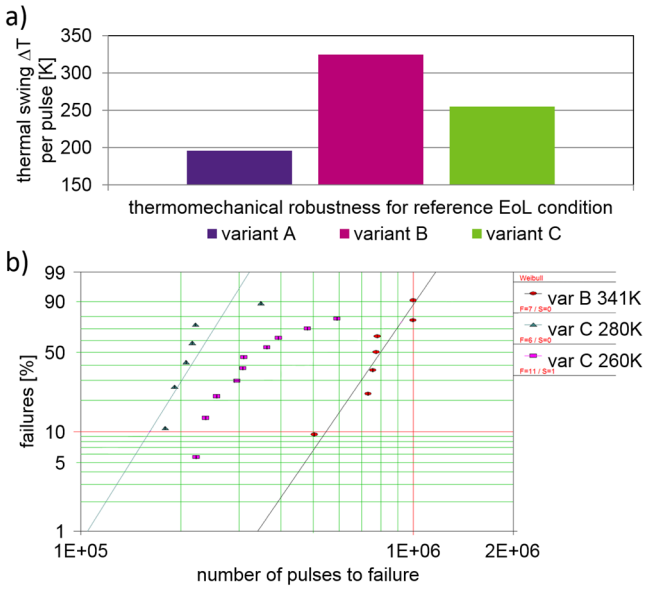

Figure 5. (a) Minimal amount of thermal swing ΔT per pulse for the three BEOL stack variants, necessary to reach similar mean number of pulses to failure (#PtF) in RPP test. (b) Weibull distribution of representative trials of stack B and C in the range of the reference #PtF.

In particular, variant B is capable to endure power pulses with ΔT ~ 340K and peak temperature of ~370K. We note that this high peak temperature is well inside the electrothermal save operating area of the device, as known from measurements and simulation (see fig. 2), such that the trials still address RPP wearout of the drivers BEOL. Failure distribution of a respective trial is shown in fig. 5b exhibiting a Weibull slope of 5 in good agreement to the trials of stack A. For stack B again we find a CM-trend to hold with CM-exponent in the range of 8.

As described in the previous section, compare fig. 3, the three stacks vary in the thicknesses of the main AlCu layers and in the Ti/TiN barrier scheme yielding the reactive or non-reactive stack. The substantially lower robustness of stack A under RPP stress we attribute mainly to the higher thickness of uppermost AlCu layer, i.e. the layer below the top copper routing layer. Smorodin et al. used nanoindentation measurements to show that critical yield stress and hardening behavior of Al thin films increases significantly for decreasing thin film thickness and demonstrated beneficial effect of additional internal TiN barriers on RPP robustness of thick Al metals [22]. For our stack variant A, thus the uppermost thicker AlCu metal layer forms a weak link for the thermomechanical robustness of the whole BEOL.

Although stack C still performs better than stack A, obviously the reactive Ti-Al stack has a detrimental effect on the thermomechanical robustness of the BEOL stack. The corresponding thermal swing to reach mean EoL after 1M pulses is in the range of 250K, about 25% lower than stack B. For stack B, too, mean RPP lifetime increases with decreasing ΔT. However, for stress with ΔT ~ 270K and below the behavior of the DUTs with BEOL variant C apparently changes, compare fig. 5b: For the trial with ΔT = 280K again EoL occurs with quite steep Weibull slope ~5. But for slightly reduced pulse power EoL distribution becomes more widely distributed, and for these trials several DUTs have been suspended without failure after 10M power pulses. Although we still have to validate this trend by further trials at lower stress level, the failure mechanism seems to change for stack B when staying below a thermal swing of 270K or peak temperature below 300°C, respectively. Small sample to sample variation like, e.g., the effective V_{DS}-clamp voltage of Zener-diode stack, might lead to observed behavior of either early failure or much higher endurance times of the samples. Based on failure analysis we discuss possible root-cause for the effect of reactive stack in the next section.

IV. Failure Analysis and Discussion

By failure analysis samples of BEOL reactive stack variant C have been studied in comparison to non-reactive stack B to clarify reasons for the weaker robustness found for the reactive stack. A set of DUTs for each stack type has been prepared at different lifetime states for cross section analysis with a focus ion beam (FIB) system. Unless otherwise stated, the scanning electron microscopy (SEM) images discussed in the following show the FIB cut (1) indicated in fig. 2a. We concentrate on the upper AlCu metals close to the thick top-metal. Here previous experiments and simulations show the largest thermomechanical stress effects [3], [11] and worst degradation is expected.

Based on the known mean number of pulses to failure (#PtF) from Weibull distribution we stressed the DUTs with pulses of ΔT = 280K (T_{max} ~ 310°C) and stopped the tests at increasing nominal lifetime state of 0% #PtF (fresh device), ~40% #PtF, ~75% #PtF, and 100% #PtF (failed device). Because of the greater RPP robustness of the non-reactive stack B, respective DUTs withstand approx. 10x more pulses compared to those of stack C for same nominal lifetime state.

For reference, the images (I.nr) and (I.r) in fig. 6 upper row show the metal levels of a fresh device before RPP stress. Compared to the non-reactive stack (I.nr), the metal lines of the reactive stack (I.r) indicate a strong formation of $TiAl_3$ grains, formed due to an annealing step after every metal level deposition. For the uppermost Al layer the $TiAl_3$ grains form on the lower surface, only, because here upper interface uses no Ti interlayer. The grains extend up to 200nm and protrude clearly into the metal layer due to aluminum consummation during annealing.

The following images in fig. 6 row II to III have been taken on samples after RPP stress. Generally, for both stacks we see a high structural robustness against fast thermal cycling. Apart from voids observed in the uppermost metal layer (see discussion below), we cannot detect systematic changes in the thickness of the metals or delamination/cracks of the interfaces between AlCu-film, barrier-layers, dielectrics, or tungsten plugs. For comparison, a significant local thickness increase as a result from RPP stress we see for the uppermost thicker AlCu layer of stack A (not shown), and this is observed in previous works, too [6]. Here the thinner metals of stack B and C for the given layout configuration do not show this obvious permanent deformation in spite of high thermal swing. Integrity of tungsten via arrays is completely unaffected as well, so catastrophic damage observed by Zhang et al. for kelvin-via structures [23] is unlikely to occur for our driver stages. Note that the images in row III taken at DUTs after failure by drain-source short in metals do not correspond to the failure site of the DUTs itself.

The behavior of Ti/TiN-Al film system under RPP stress becomes visible when comparing images for stack B and C in fig. 6: For DUTs with a stress load of 40% (II.nr) and 50% #PtF (II.r), respectively, a drift of $TiAl_3$ grains through the AlCu film is observed. In case of the reactive stack, the $TiAl_3$ grains become more widely distributed but smaller, whereas for the non-reactive stack the grains keep their size and number. Ultimately, for a failed DUT of stack C, fig. 6 image III.r, the $TiAl_3$ grains are out-diffused widely connecting the top and bottom $TiAl_3$ coat of the metal level, in particular observable for the lower metal layer shown in the image.

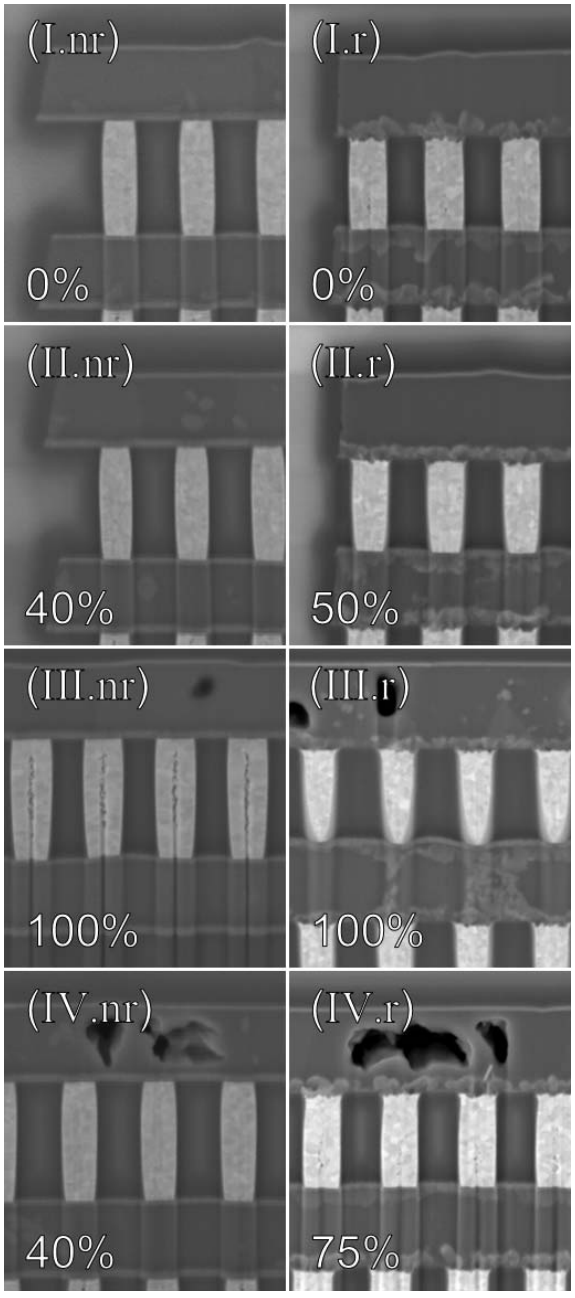

Figure 6. SEM images of cross sections of the upper part of the aluminum stack of four DUTs of BEOL variant B (left col 'nr') and C (right col 'r'). Relative stress load w.r.t. mean #PtF is indicated in the lower right corner of the image. The cross sections in row I to III are images of FIB cut (1) (comp. fig. 2a) and row IV contains images of FIB cut (2).

The images fig. 6, row I to III, discussed so far, show cross sections at the position of FIB cut (1), made close to the center of the power stage structure. Here both temperature and current density in the lower metal levels reach the highest values, compare fig. 2. For comparison in fig. 6 row IV two cross sections for non-reactive and reactive stack with medium stress load level (40% and 75% #PtF) are shown taken at position of FIB cut (2), between power stage center and edge (see fig. 2a). At this position, lateral temperature gradient is largest while current density in the lower metal levels is less than 40% compared to center position. The general observations, i.e. good integrity of interfaces and unchanged metal thickness, hold for the stressed BEOL stacks at this position as well. In comparison to the previous images, however, we find significant voids formed in the lower thin AlCu metal level.

As driving mechanism for formation of these voids, generally both EM and migration due to the thermomechanical stress from RPP operation may be considered. In particular, a high lateral thermal gradient may lead to material migration and correlation of RPP failure sites with those positions has been reported [6], [11]. For the present structures, we attribute the voids to EM effects for the following reason: Voids are present in the metal MX fingers (comp. fig. 3) at position cut (2) which are connected through top-vias to the power metal. Directly neighboring metal lines with the comparable thermomechanical stress load but without top-via contacts do not form such voids. So local current source/sink at top via connection most probably lead to voiding in the MX layer, while lateral current flow alone, even at position of cut (1) with higher temperature and current density, does not lead to pronounced EM effects for our cumulated load from stress trials.

In our context we have to make sure, that device failure occurs through aging under RPP stress and EM effects -if relevant- are not lifetime limiting. Here EM and in particular buildup of metal voids prominently in MX we do not consider to be relevant for EoL in our trials, since: -a- failure sites do not correlate to observed voiding effects, -b- images IV.nr and IV.r show comparable voiding but the samples with non-reactive stack exhibit almost 10x RPP lifetime, and -c- RPP EoL changes with CM-exponent larger 5. The last point implies that a small, e.g. 20%, change in current value giving a roughly proportional change in ΔT leads to a large change in RPP lifetime, which is not expected from Black's equation alone.

In summary, we find a detrimental effect of the $TiAl_3$ grains -present when using a reactive stack- on the thermomechanical robustness of the AlCu BEOL for fast thermal cycling with high temperature excursion. Instability of the Ti-Al alloy has been observed in pulsed EM test as well leading to a pronounced effect on sheet resistance [24]. In our case, the high temperature excursion together with connected stress gradients may lead to a pronounced drift of the grains through the AlCu film. These structural changes are also observed for metal lines present in the power stage routing without actual current load, so again EM effects can be excluded. We suppose that the $TiAl_3$ grain drift leads to additional mechanical stress on AlCu grain interfaces of the bamboo structure. Thereby the mechanical and electrical material properties are changed locally leading to weak spots, which may initiate or accelerate, respectively, a catastrophic crack in dielectric leading to a short in the metallization system.

V. CONCLUSIONS

The thermomechanical robustness of the AlCu smart-power backend is not only determined by the dimensions of metal layers and the associated yield stress (basically given by the general corresponding technology node), it is also decisively influenced by the detailed Ti-Al(Cu) backend layer sequence, generating a reactive or non-reactive stack. For our half-reactive reference stack including a thicker uppermost AlCu layer we can model RPP-aging over five orders of magnitude in lifetime by an extended Coffin-Manson approach, allowing straightforward derivation of design guidelines for different RPP mission profiles. For the two additional BEOL variants with lower AlCu thickness this model applies too, yielding higher lifetime, but this trend has to be confirmed by trials with higher pulse number. Stressed under accelerated conditions, the test samples of reactive stack show lower lifetime compared to non-reactive stack and a drift of $TiAl_3$ grains through the AlCu film is observed in failure analysis as the only relevant finding different to the two stacks. We attribute this effect to be responsible for the lower robustness of a reactive stack under RPP stress. In summary, the highest RPP robustness is obtained using a stack of thin AlCu metal layers formed by a non-reactive stack. Considering current capability with respect to EM lifetime limits this is the weakest option, and such a BEOL stack might indeed hamper realization of output drivers in smart-power applications, if usage of additional lower metal layers for routing shall be avoided.

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REFERENCES

[1] D. Disney und Z. J. Shen, „Review of Silicon Power Semiconductor Technologies for Power Supply on Chip and Power Supply in Package Applications," *IEEE Transactions on Power Electronics,* Bd. 28, Nr. 9, pp. 4168-4181, Sept 2013.

[2] M. Rose und H. J. Bergveld, „Integration Trends in Monolithic Power ICs: Application and Technology Challenges," *IEEE Journal of Solid-State Circuits,* Bd. 51, Nr. 9, pp. 1965-1974, Sept 2016.

[3] F. Pozzobon, D. Paci, G. Pizzo, A. Buri, S. Morin, F. Carace, A. Andreini, D. Gastaldi, E. Bertarelli, R. Lucchini und P. Vena, „Reliability characterization and FEM modeling of power devices under repetitive power pulsing," in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, 2013.

[4] W. Kanert, „Reliability challenges for power devices under active cycling," in *2009 IEEE International Reliability Physics Symposium*, 2009.

[5] D. Martineau, C. Levade, M. Legros, P. Dupuy und T. Mazeaud, „Universal mechanisms of Al metallization ageing in power devices," *Microelectronics Reliability ,* Bd. 54, Nr. 11, pp. 2432-2439, 2014.

[6] T. Smorodin, J. Wilde, P. Alpern und M. Stecher, „A Temperature-Gradient-Induced Failure Mechanism in Metallization Under Fast Thermal Cycling," *Device and Materials Reliability, IEEE Transactions on,* Bd. 8, Nr. 3, pp. 590-599, Sept 2008.

[7] H. Nguyen, C. Salm, J. Vroemen, J. Voets, B. Krabbenborg, J. Bisschop, A. Mouthaan und F. Kuper, „Fast temperature cycling and electromigration induced thin film cracking in multilevel interconnection: experiments and modeling," *Microelectronics Reliability ,* Bd. 42, Nr. 9-11, pp. 1415-1420, 2002.

[8] C. Kendrick, R. Stout und M. Cook, „Reliability of NLDMOS transistors subjected to repetitive power pulses," in *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, 2008.

[9] F. Meier, C. Schwarz und E. Werner, „Crystal-plasticity based thermo-mechanical modeling of Al-components in integrated circuits," *Computational Materials Science ,* Bd. 94, pp. 122-131, 2014.

[10] D. Simon, C. Boianceanu, G. De Mey und V. Topa, „Experimental Reliability Improvement of Power Devices Operated Under Fast Thermal Cycling," *Electron Device Letters, IEEE,* Bd. 36, Nr. 7, pp. 696-698, July 2015.

[11] M. Ritter, G. Pham und M. Pfost, „On-Chip Sensors to Detect Impending Metallization Failure of LDMOS Transistors Under Repetitive Thermo-Mechanical Stress," *IEEE Transactions on Semiconductor Manufacturing,* Bd. 29, Nr. 3, pp. 193-200, Aug 2016.

[12] M. Pfost, D. Costachescu, A. Podgaynaya, M. Stecher, S. Bychikhin, D. Pogany und E. Gornik, „Small embedded sensors for accurate temperature measurements in DMOS power transistors," in *Microelectronic Test Structures (ICMTS), 2010 IEEE International Conference on*, 2010.

[13] M. Ershov, A. Tcherniaev, Y. Feinberg, P. Lindorfer, W. French und P. Hopper, „Numerical simulation of metal interconnects of power semiconductor devices," in *Power Semiconductor Devices IC's (ISPSD), 2010 22nd International Symposium on*, 2010.

[14] A. Mann, H. Lohmeyer und Y. Joseph, „Low-cycle fatigue of multilayer metal stack employed as fast wafer level monitor for backend integrity in smart power technologies," in *2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2016.

[15] G. V. den bosch, P. Moens, P. Gassot, D. Wojciechowski und G. Groeseneken, „Analysis and application of energy capability characterization methods in power MOSFETs," in *Proceedings of the 30th European Solid-State Circuits Conference*, 2004.

[16] M. Glavanovics, H. Köck, V. Kosel und T. Smorodin, „Flexible active cycle stress testing of smart power switches," *Microelectronics Reliability ,* Bd. 47, pp. 1790-1794, 2007.

[17] J. J. Estabil, H. S. Rathore und E. N. Levine, „Electromigration improvements with titanium underlay and overlay in Al(Cu) metallurgy," in *VLSI Multilevel Interconnection Conference, 1991, Proceedings., Eighth International IEEE*, 1991.

[18] C. D. Graas, H. A. Le, J. W. McPherson und R. H. Havemann, „Electromigration reliability improvement of W-plug vias by titanium layering," in *Proceedings of 1994 IEEE International Reliability Physics Symposium*, 1994.

[19] K. Norris und A. Landzberg, „Reliability of Controlled Collapse Interconnections," *IBM Journal of Research and Development,* Bd. 13, Nr. 3, pp. 266-271, May 1969.

[20] K. Hiraoka, „Elastoplastic creep analysis of thermal stress and strain in aluminum interconnects of LSIs," *Electronics and Communications in Japan (Part II: Electronics),* Bd. 77, Nr. 3, pp. 93-105, 1994.

[21] J. McPherson, Reliability Physics and Engineering: Time-To-Failure Modeling, Springer Science+Business Media, 2010.

[22] T. Smorodin, J. Wilde, P. Nelle, E. Lilleodden und M. Stecher, „Modeling of DMOS subjected to fast temperature cycle stress and improvement by a novel metallization concept," in *Reliability Physics Symposium, 2008. IRPS 2008. IEEE International*, 2008.

[23] M. Zhang, Y. Yoshihisa, K. Furuya, Y. Imai, K. Hatasako, T. Ipposhi und S. Maegawa, „Reliability study of thermal cycling stress on smart power devices," *Japanese Journal of Applied Physics,* Bd. 53, Nr. 4S, p. 04EP12, 2014.

[24] A. Ferrara, J. Claes, M. Swanenberg, L. van Dijk und P. G. Steeneken, „Accelerated resistance degradation in aluminum by pulsed power cycling," in *Power Semiconductor Devices IC's (ISPSD), 2015 IEEE 27th International Symposium on*, 2015.